



PTO/SB/08A (08-03)

Substitute for form 1449A/PTO		Complete if Known			
		Application Number	10/645,788		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Filing Date	August 20, 2003		
		First Named Inventor	Maangat, Simar		
		Art Unit	2855		
		Examiner Name	To Be Assigned		
		Attorney Docket Number	015114-067800US		
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U.S. PATENT DOCUMENTS+					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Kind Code ² (if known)			
ml	0001	US-4,719,369	01-12-1988	Asano et al.	
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	0003	US-5,111,081	05-05-1992	Atallah	
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Examiner Signature	<i>Don</i>	Date Considered	<i>10/14/04</i>
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	0035	US-6,362,644 B1	03-26-2002	Jeffrey et al.	
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	0040	US-6,433,579 B1	08-13-2002	Wang et al.	
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	0049	US 2002/0010853 A1	01-24-2002	Trimberger et al.	
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	0051	US 2002/0101278 A1	08-01-2002	Schultz et al.	
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Examiner Initials*	Cite No. ¹	Foreign Patent Document			Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ²
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Examiner Signature	<i>[Signature]</i>	Date Considered	10/14/04
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NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
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	0058	Esch and Manley, Theory and Design of CMOS HSTL I/O Pads, The Hewlett Packard Journal, Aug. 1998	/
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	0061	Xilinx, "Virtex-II Platform FPGAs: Detailed Description," Xilinx, DS031-2 (v3.1) October 14, 2003	/
he	0062	Xilinx, "Virtex-II Pro Platform FPGAs: Functional Description," Xilinx, DS083-2 (v2.9) October 14, 2003	/

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